CLAIMS

What is claimed is:

1. A chip reactor comprising a carrier having at least two different microreaction channels, each of the channels comprising at least one reaction space, at least one inlet and at least one outlet, wherein each of the channels is suitable for operation independent of the other.

2. The chip reactor according to claim 1, wherein the carrier comprises a silicon/glass composite.

3. The chip reactor according to claim 2, wherein at least a portion of the channels is etched.

4. The chip reactor according to claim 2, wherein at least a portion of the at least one reaction space is coated with silicon dioxide.

5. The chip reactor according to claim 4, wherein the silicon dioxide has a thickness of from 50 to 2000 nm.

6. The chip reactor according to claim 1, wherein the carrier has from 2 to 100 different microreaction channels, each of the channels comprising at least one reaction space, at least one inlet and at least one outlet, wherein each of the channels is suitable for operation independent of the other.

7. The chip reactor according to claim, 1, wherein each of the reaction spaces comprises a channel having a length of from 1 to 500 mm.

8. The chip reactor according to claim 1, wherein the reaction spaces have one or more mixing points.

9. The chip reactor according to claim 1, wherein at least one of the channels has at least two inlets, the at least two inlets impinging on each other at a mixing angle of from 15° to 270°.

10. The chip reactor according to claim 1, wherein at least one of the reaction spaces has one or more mixing points.

11. The chip reactor according to claim 1, wherein the chip reactor is divided into two or more zones for variable processing.

12. The chip reactor according to claim 11, wherein the two or more zones can be heated/cooled independently of one another.

13. The chip reactor according to claim 1, wherein the carrier is embedded in a manifold having an inbound passageway corresponding to the at least one inlet and an outbound passageway corresponding to the at least one outlet.

14. The chip reactor according to claim 13, wherein the manifold comprises an inert material.

15. The chip reactor according to claim 13, wherein the manifold further comprises at least one passageway for a heat transfer liquid.

16. The chip reactor according to claim 13, wherein the manifold further comprises a facility for visual inspection of the chip reactor.

17. The chip reactor according to claim 13, further comprising a seal separating the chip reactor from the manifold.

18. The chip reactor according to claim 1, wherein the carrier has at least three different microreaction channels, each of the channels comprising at

least one reaction space, at least one inlet and at least one outlet, wherein each of the channels is suitable for operation independent of the other.

19. The chip reactor according to claim 1, wherein the carrier has from 5 to 50 different microreaction channels, each of the channels comprising at least one reaction space, at least one inlet and at least one outlet, wherein each of the channels is suitable for operation independent of the other.

20. A chip reactor comprising a silicon/glass composite carrier having from 5 to 50 different microreaction channels etched therein, each of the channels comprising at least one reaction space, a portion of which is coated with silicon dioxide having a thickness of from 50 to 2000 nm, at least one inlet and at least one outlet, wherein each of the channels is suitable for operation independent of the other, and wherein the carrier is embedded in an inert manifold having an inbound passageway corresponding to each inlet, an outbound passageway corresponding to each outlet, at least one passageway for a heat transfer liquid and a facility for visual inspection of the chip reactor.